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4 SEM TDC PHYH (CBCS) C 10

2024

(May/June)

PHYSICS

(Core)

Paper : C–10

(Analog Systems and Applications)

Full Marks : 53
Pass Marks : 21

Time : 3 hours

The figures in the margin indicate full marks for the questions

1. Choose the correct option : 1×5=5

(a) The width of the depletion layer of a junction

(i) is independent of applied voltage

(ii) is increased under reverse bias

(iii) decreases with light doping

(iv) increases with heavy doping

(b) The colour of the emitted light of LED depends on the

(i) construction method

(ii) applied voltage

(iii) energy gap of the material used

(iv) None of the above

(c) In RC coupled amplifier, voltage gain over mid-frequency range

(i) is increasing

(ii) is constant

(iii) is decreasing

(iv) is zero

(d) Oscillators employ

(i) negative feedback

(ii) no feedback

(iii) positive feedback

(iv) None of the above

(e) Open-loop voltage gain of OP-AMP

(i) is small

(ii) is large

(iii) is zero

(iv) None of the above

2. (a) What happens to the depletion region of junction diode under forward and reverse bias condition? Explain. 3

Or

Define Fermi level in a semiconductor. How does its position change when (i) donor and (ii) acceptor are added to the semiconductor? 1+1+1=3

(b) Derive an expression for the width of depletion layer of a *p-n* junction diode. 4

Or

Define the mobility of charge carriers and conductivity. What is the effect of temperature on the conductivity of a semiconductor?

3. *(a)* Explain with circuit diagram the action of Zener diode as a voltage regulator. 3

(b) Write about working and construction of photovoltaic cell. 2

4. *(a)* What do you mean by quiescent point or Q-point? What is the best position of Q-point on the DC load line in the transistor characteristics? 2

(b) Explain active region, saturation region and cut-off region in transistor operation. 3

Or

The collector leakage current in a transistor is 300 μA in CE arrangement. If the transistor is now connected in the CB arrangement, what will be the leakage current? Given $\beta = 100$.

5. *(a)* Draw a circuit for voltage-divider bias method. What are its advantages and disadvantages? 1+2=3

(b) Derive expression for the current gain and the voltage gain of a single-stage common-emitter transistor amplifier using *h*-parameters. 3

(c) A CE transistor amplifier is connected with a load resistance 2 kΩ. If the *h*-parameters of the transistor are $h_{ie} = 1000\ \Omega$, $h_{re} = 10^{-4}$, $h_{fe} = 100$ and $h_{oe} = 12 \times 10^{-6}$ S, find the current gain, input impedance and voltage gain. 2

6. *(a)* Draw the circuit diagram of an RC coupled transistor amplifier and give its mid-frequency equivalent circuit. Derive an expression for gain at the mid-frequency range. 2+2=4

(b) What is non-linear distortion? How can it be minimized? 1+2=3

(c) Calculate the Barkhausen's criterion for self-sustained oscillations. 3

Or

An RC phase-shift oscillator has the parameter values $R_L = 3{\cdot}3$ kΩ, $R = 5{\cdot}6$ kΩ and $C = 0{\cdot}01$ μF. Calculate frequency of oscillations and the h_{fe} required for sustaining the oscillations.

7. *(a)* Draw the basic non-inverting amplifier with an input resistance R_1 and a feedback resistance R_f. Assuming the OP-AMP to be ideal, derive the expression for the voltage gain of the non-inverting amplifier. 1+3=4

Or

Calculate the CMRR of OP-AMP. 4

(b) Explain with circuit diagram of an OP-AMP as integrator. 3

Or

The input to the differentiator OP-AMP is a sinusoidal voltage of peak value 10 mV and frequency 2 kHz. Find the output, if $R = 200\ k\Omega$ and $C = 2\ \mu F$.

(c) Explain the significance of virtual ground of a basic inverting amplifier. What do you understand by closed-loop and open-loop voltage gain of an OP-AMP? 3

Or

Consider the inverting OP-AMP with $R_1 = 10\ k\Omega$, $R_f = 100\ k\Omega$, $V_{in} = 1\ V_{pp}$ and power supply voltages ± 18 V. Find *(i)* closed-loop voltage gain and *(ii)* the maximum operating frequency. The slew rate is 0·5 V/μs.

(Continued)

8. Explain the working of a binary weighted-resistor network. 3

Or

Briefly describe the resolution (step size) and accuracy specifications of a D/A converter.

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