Total No. of Printed Pages—7

4 SEM TDC PHYH (CBCS) C 10

2022

(June/July)

PHYSICS

(Core)

Paper : C–10

(Analog Systems and Applications)

Full Marks : 53
Pass Marks : 21

Time : 3 hours

The figures in the margin indicate full marks for the questions

1. Choose the correct answer : 1×5=5

(a) When reverse bias is applied to a junction diode

(i) width of depletion layer decreases

(ii) potential barrier increases

(iii) potential barrier decreases

(iv) minority carrier increases

(b) The rectification efficiency of full-wave rectifier is _____ of half-wave rectifier.

(i) equal

(ii) half

(iii) double

(iv) 1·21 times

(c) Quiescence is a state of

(i) activity

(ii) inactivity

(iii) amplification

(iv) switching

(d) In a transistor amplifier, the input impedance should be

(i) low

(ii) high

(iii) negligible

(iv) None of the above

(e) Which of the following electrical characteristics is not exhibited by an ideal OP-AMP?

(i) Infinite voltage gain

(ii) Infinite bandwidth

(iii) Infinite output resistance

(iv) Infinite slew rate

2. (a) Explain how depletion layer is formed under unbiased situation of a *p-n* junction diode. 3

(b) Explain the current flow mechanism in forward and reverse biased *p-n* junction diode. 4

Or

Define the mobility of charge carriers and conductivity. Obtain an expression for the electrical conductivity of an intrinsic semiconductor. 1+3=4

3. *(a)* Explain with circuit diagram, the Zener diode as a voltage regulator. 3

(b) Describe the working of LED. 2

4. *(a)* Draw the C-E circuit of a transistor. Sketch its output characteristics. Explain the active, cut-off and saturation regions. 1+1+2=4

(b) Define α and β of a transistor. Write the relation between them. 2

5. *(a)* Draw a voltage-divider bias circuit and derive an expression for its stability factor. 4

Or

A germanium transistor with $\beta = 100$ is to be operated as a C-E amplifier with fixed bias method. The transistor operates at the signal collector current $I_C = 1$ mA and $V_{CE} = 4$ V. If a load resistance of 2 kΩ is connected in the collector circuit, then find the base resistance to be connected. (For germanium transistor $V_{BE} = 0 \cdot 3$ V)

(b) Draw the small signal hybrid equivalent circuit of a common-emitter transistor amplifier and derive the expressions for current gain and input impedance. 4

Or

Explain class *A*, class *B* and class *C* amplifiers with graphical representation.

6. Draw and discuss the frequency response curve of an *R-C* coupled transistor amplifier showing cut-off frequencies and the bandwidth. 3

7. Discuss the effect of negative feedback on the input and output impedances of an amplifier. 3

8. State Barkhausen's criterion and explain the conditions that must be satisfied for feedback amplifier to produce steady oscillations. 1+2=3

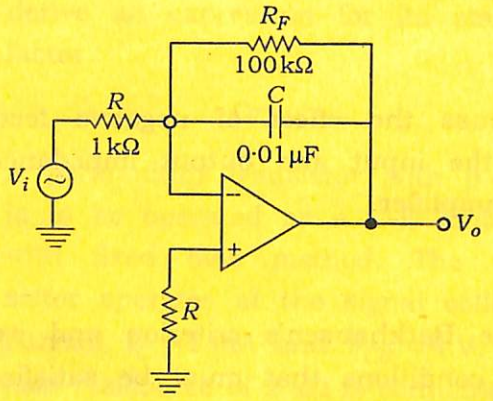
Or

Draw circuit diagram of an *R-C* phase shift oscillator and explain its operation. 3

9. *(a)* What is an OP-AMP? Draw the schematic block diagram of basic OP-AMP. 1+2=3

(b) Explain with circuit diagram, the adder and subtractor using OP-AMP. 4

(c) Determine the lower frequency limit (critical frequency) for the integrator circuit shown below : 3



Or

Discuss OP-AMP as log amplifier.

(Continued)

10. Draw the block diagram of successive approximation type A/D converter. 3

Or

Draw the circuit diagram of weighted resistor type D/A converter.

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