4 SEM TDC PHYH (CBCS) C 10

2023

(May/June)

PHYSICS

(Core)

Paper : C–10

(Analog Systems and Applications)

Full Marks : 53

Pass Marks : 21

Time : 3 hours

The figures in the margin indicate full marks for the questions

1. Choose the correct answer : 1×5=5

(a) Under forward bias, current in a *p-n* diode does not flow before it attains _____ in silicon and germanium *p-n* junction diode respectively.

(i) 0·5 V and 0·7 V

(ii) 0·7 V and 0·3 V

(iii) 1·1 V and 0·7 V

(iv) 0·3 V and 0·7 V

(b) Avalanche breakdown is primarily dependent on the phenomenon of

(i) doping

(ii) ionisation

(iii) recombination

(iv) collision

(c) The value of α of a transistor is

(i) more than 1

(ii) less than 1

(iii) 1

(iv) 0

(d) In CE arrangement, the value of input impedance is approximately equal to

(i) h_{ie}

(ii) h_{oe}

(iii) h_{re}

(iv) None of the above

(e) Which of the following amplifiers cannot be used for audio frequency amplifier?

(i) Class A

(ii) Class B

(iii) Class AB

(iv) Class C

2. (a) Draw the energy band diagrams of *n*-type and *p*-type semiconductors indicating the position of Fermi level. 3

Or

Distinguish between static and dynamic resistance of a *p-n* junction diode. Do they depend on temperature and bias voltage? 2+1=3

(b) Explain the formation of barrier potential in a *p-n* junction. Derive an expression for the barrier potential of a *p-n* junction. 4

Or

Discuss different types of *p-n* junction diodes on the basis of method of fabrication.

3. *(a)* Draw the circuit diagram of a full-wave rectifier and calculate its ripple factor. 1+2=3

(b) Write about the working and construction of a photodiode. 2

4. *(a)* What is a load line in the transistor characteristics? Explain its significance. 2

(b) Explain with necessary diagram, the mechanism of current flows in an *n-p-n* transistor. 3

Or

A load resistance of 4 kΩ is connected in collector circuit of a common emitter transistor amplifier with $V_{CC} = 12$ V. What are the cut-off point and saturation point of output characteristics of the amplifier? Find the coordinate of the operating point, if the zero signal base current is 20 μA and $\beta = 100$. 5

5. *(a)* Draw a fixed bias circuit. On the basis of stability factor, mention the merits and demerits of this circuit. 2+1=3

(b) Starting from the two equations for the hybrid parameters, draw the *h*-parameter equivalent circuit for a common emitter transistor circuit. 3

(c) In CE transistor amplifier, following current and voltages are found :

(i) When output ac is short-circuited, $I_b = 20$ μA, $I_c = 2$ mA, $V_{be} = 20$ mV

(ii) When input ac is open-circuited, $V_{bc} = 0{\cdot}75$ mV, $I_c = 90$ μA, $V_{ce} = 1{\cdot}5$ V Find the *h*-parameters of the transistor. 2

6. *(a)* Explain the operation of a two-stage RC coupled CE transistor amplifier with a neat circuit diagram. 2+2=4

(b) What is negative feedback? Explain with necessary frequency response curve, how the bandwidth of an RC coupled amplifier is modified when negative feedback is used. 1+2=3

(c) Describe a Hartley or a Colpitts oscillator circuit and explain its operation. 3

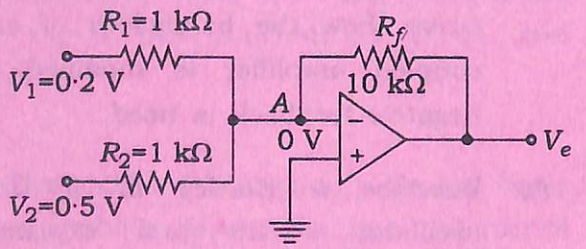
7. *(a)* Draw the basic inverting amplifier with an input resistance R_1 and a feedback resistance R_f. Assuming the OP-AMP to be ideal, derive the expression for the voltage gain of the inverting amplifier. 2+2=4

(b) Explain with circuit diagram of an OP-AMP as differentiator. 3

(c) Define CMRR and slew rate of an OP-AMP. What is the importance of CMRR? 2+1=3

Or

Determine the output voltage for the summing amplifier as shown below : 10



8. What is the function of a DAC? Write the advantage of the R-2R ladder type DAC over the weighted-resistor type DAC. 1+2=3

Or

Design a 4-bit weighted-resistor DAC whose full-scale output voltage is – 5 V. The logic levels are 1 = + 5 V and 0 = 0 V. What is the output voltage, when the input is 1101? 3

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